WHAT IS CLAIMED IS:

1. An information processing system comprising:

a processor;

a memory; and

a memory controller connected with said processor via a first bus and connected with said memory via a second bus for controlling said memory,

wherein said memory controller comprises a buffer memory and a control circuit, and said control circuit is controlled, before a memory access is carried out from said processor, to estimate an address to be possibly next accessed on the basis of addresses accessed in the past and to prefetch data stored in said memory into said buffer memory, in accordance with said estimated address wherein said data has a data size of twice or more an access unit of said processor.

2. An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough; said control circuit, when the access from said processor hits data within said buffer memory, is controlled to transfer the data to said processor, whereas, said control circuit, when the access from said processor fails to hit data within said buffer memory, is controlled to transfer data within said memory to said processor via said direct path.

3. An information processing system according to

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claim 1, wherein said memory stores an instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer memory.

4. An information processing system according to claim 1, wherein said memory stores therein an instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and operand data into said buffer memory.

5. An information processing system according to claim 1, comprising a plurality of buffer memories into which data of said access unit is prefetched, and wherein said control circuit controls to transfer data already stored in said plurality of buffer memories to said processor in an order different from an address order.

6. An information processing system according to claim 1, wherein said memory controller has an instruction decoder and a branching buffer memory, and said control circuit, when said instruction decoder detects a branch instruction, prefetches an instruction code as a branch destination into said branching buffer memory and, when an access is made from said processor to the instruction code, judges whether or not the instruction code hits data within said buffer memory and said branching buffer memory.

7. An information processing system according to claim 1, wherein said memory controller has a register

for instructing start or stop of the prefetch to said buffer memory.

8. An information processing system according to claim 1, wherein said control circuit is controlled in its initial state to prefetch data already stored at a pre-specified address into said buffer memory.

9. An information processing system according to claim 1, wherein said control circuit is controlled, when the access from said processor fails to hit data within said buffer memory, to transfer data from said processor to said memory through said direct path and also to clear data within said buffer memory to perform read-ahead operation to said buffer memory.

10. An information processing system according to claim 1, wherein said control circuit is controlled, when the access from said processor hits said buffer memory and when a size of the data already stored in said buffer memory is equal to or smaller than said access unit, to prefetch the data into said buffer memory until the buffer memory becomes full of the data and, when the access from said processor fails to hit said buffer memory, to clear the data within said buffer memory to prefetch the data until said buffer memory becomes full of the data.

11. An information processing system according to claim 1 wherein said processor has an internal cache, and said control circuit is controlled to prefetch data having a data size of twice or more a line size of said

internal cache into said buffer memory.

12. An information processing system according to claim 1, wherein said memory is divided into a first memory for storing therein an instruction code to be executed on said processor and a second memory for storing therein operand data; said memory controller has an access judgement circuit for judging whether the access from said processor is an access to said first memory or an access to said second memory, a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and said control circuit is controlled to prefetch the instruction code into said first buffer memory according to an judgement of said access judgement circuit or to prefetch the operand data into said second buffer memory.

13. An information processing system comprising:

a processor;

a memory; and

a memory controller connected to said processor via a first bus and also connected to said memory via a second bus,

wherein said memory controller comprises a buffer memory and a control circuit for controlling to prefetch data within said memory into said buffer memory, said memory and said controller are mounted on an identical chip, and an operational frequency of said second bus is higher than that of said first bus.

14. An information processing system according to

claim 13, wherein said control circuit is controlled, before a memory access from said processor is carried out, to estimate an address to be possibly next accessed on the basis of addresses accessed in the past and to prefetch data stored in said memory into said buffer memory in accordance with said estimated address, wherein said data has a data size of twice or more an access unit of said processor.

15. An information processing system comprising:

a processor;

a memory; and

a memory controller connected to said processor via a first bus and also connected to said memory via a second bus,

wherein said memory controller comprises a buffer memory and a control circuit for controlling to prefetch data within said memory into said buffer memory, said memory and said controller are mounted on an identical chip, and a bus width of said second bus is larger than that of said first bus.

16. An information processing system according to claim 15, wherein said control circuit is controlled, before a memory access from said processor is carried out, to estimate an address to be possibly next accessed on the basis of addresses accessed in the past and to prefetch data stored in said memory into said buffer memory in accordance with said estimated address, wherein said data has a data size of twice or more an access unit

of said processor.

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